WHAT IS CLAIMED IS:

1. A semiconductor storage device in which only a defective element is replaced by a row redundant element to compensate for a defect if at least one of a plurality of elements is defective in a case where the plurality of elements in a cell array unit are simultaneously activated, comprising:

an array control circuit which is configured to interrupt the operation of the defective element by preventing a word line state signal from being received based on a signal to determine whether a row redundancy replacement process is performed or not,

wherein the word line state signal is input to the plurality of memory blocks in the cell array unit via a single signal line.

2. A semiconductor storage device in which only a defective element is replaced by a row redundant element to compensate for a defect if at least one of a plurality of elements is defective in a case where the plurality of (2^n: n is a natural number) elements in a cell array unit are simultaneously activated, comprising:

n signal lines which transmit signals representing any one of the elements to be activated simultaneously, when is found to be defective and which should be replaced by a row redundant element: and

an array control circuit configured to locally

decode signals transmitted via said n signal lines, and set an element selected in the plurality of elements into a disable state.

3. A semiconductor storage device in which only a defective element is replaced by a row redundant element to compensate for a defect if at least one of a plurality of elements is defective in a case where the plurality of (2^n: n is a natural number) elements in a cell array unit are simultaneously activated, comprising:

a first signal line which transmits a word line state signal indicating activation and deactivation of the plurality of elements,

a second signal line which transmits a signal indicating occurrence of redundancy replacement of the defective element by the row redundant element,

n third signal lines which transmit signals having address information indicating which one of the plurality of elements to be activated simultaneously is replaced at the time of replacement of the defective element by the row redundant element if at least one of the plurality of elements is defective, and

an array control circuit which is configured to decode the signals transmitted via the n third signal lines for each memory block,

wherein the row redundant element is set into an activated state and the defective element is set into

a deactivated state and replaced by the row redundant element by use of said array control circuit if at least one of the plurality of elements is defective.

4. The semiconductor storage device according to claim 3, wherein said first to third signal lines are commonly used by a plurality of memory blocks in the memory cell array.

5. The semiconductor storage device according to claim 3, further comprising a spare memory block for the redundant elements.

6. A semiconductor storage device in which only a defective element is replaced by a row redundant element to compensate for a defect if at least one of a plurality of elements is defective in a case where the plurality of elements in a cell array unit are simultaneously activated, comprising:

a control circuit configured to hold address and redundancy information in an operation mode of sequentially activating a plurality of word lines at different times, thereby to select the word lines together.

7. The semiconductor storage device according to claim 6, wherein said control circuit continuously holds the address information and redundancy information while the word line is kept activated in a case where the redundant element is selected.

8. The semiconductor storage device according to

claim 6, wherein timing for equalizing the bit lines is shifted when the plurality of word lines are precharged at one time.

9. The semiconductor storage device according to claim 6, wherein the cell array unit includes a plurality of memory blocks and M (M=2, 3, 4, 5, …) word lines are selected together in the memory block.

10. The semiconductor storage device according to claim 6, wherein an output of the control circuit controls two adjacent memory blocks.

11. A semiconductor storage device in which only a defective element is replaced by a row redundant element to compensate for a defect if at least one of a plurality of elements is defective in a case where the plurality of elements in a cell array unit are simultaneously activated, comprising:

an array control circuit which is configured to set the row redundant element into an activated state, set the defective element into a deactivated state and replace the defective element by the row redundant element if at least one of the plurality of elements is defective,

said array control circuit including

a first latch circuit configured to hold a present state until a precharge command is received if an array control circuit state signal is received in an operation mode of sequentially activating a plurality

of word lines at different times, thereby to activate the word lines together,

a second latch circuit configured to hold an activation/deactivation state of a sense amplifier,

a third latch circuit configured to hold a word line activation signal in the operation mode of sequentially activating a plurality of word lines at different times, thereby to activate the word lines together, and

a fourth latch circuit configured to hold a signal used to control the state of a row decoder.

12. The semiconductor storage device according to claim 11, wherein the cell array unit includes a plurality of memory blocks and said array control circuit is provided for each of the memory blocks.

13. The semiconductor storage device according to claim 11, wherein timing for equalizing the bit line pares is shifted when the plurality of word lines are precharged at one time.

14. The semiconductor storage device according to claim 11, wherein the cell array unit includes a plurality of memory blocks and M (M=2, 3, 4, 5, …) word lines are selected together in the memory block.

15. A semiconductor storage device in which only a defective element is replaced by a row redundant element to compensate for a defect if at least one of a plurality of elements is defective in a case where the

plurality of elements in a cell array unit are simultaneously activated, comprising:

an array control circuit which is configured to set the row redundant element into an activated state, set the defective element into a deactivated state and replace the defective element by the row redundant element if at least one of the plurality of elements is defective,

said array control circuit including

a first latch circuit configured to hold a present state until a precharge command is received if an array control circuit state signal is received in an operation mode of sequentially activating a plurality of word lines at different times, thereby to activate the word lines together,

a second latch circuit configured to hold an activation/deactivation state of a sense amplifier,

a third latch circuit configured to hold a word line activation signal in the operation mode of sequentially activating a plurality of word lines at different times, thereby to activate the word lines together, and

a control circuit configured to control the state of a row decoder.

16. The semiconductor storage device according to claim 15, wherein the cell array unit includes a plurality of memory blocks and said array control

circuit is provided for each of the memory blocks.

17. The semiconductor storage device according to claim 15, wherein timing for equalizing the bit line pares is shifted when the plurality of word lines are precharged at one time.

18. The semiconductor storage device according to claim 15, wherein the cell array unit includes a plurality of memory blocks and M (M=2, 3, 4, 5, …) word lines are selected together in the memory block.

19. The semiconductor storage device according to claim 15, further comprising a control circuit configured to control the row decoder, and an output of the control circuit is input to row decoders of two adjacent memory cell blocks.

20. A semiconductor storage device in which a plurality of word lines are activated together by causing each of the word lines which is once activated to hold the activated state through a plurality of successive word line selection cycles, comprising:

a latch circuit which is configured to fetch part of address information to specify a word line to be selected and redundancy information indicating whether the address information coincides with a previously programmed address in each word line selection cycle and activate and hold a word line activation signal used to select a word line at the time of being selected by address information in a specified cycle

and non-coincidence of redundancy.

21. The semiconductor storage device according to claim 20, wherein said latch circuit generates and holds the word line activation signal which is word line control signal used for each memory block.

22. The semiconductor storage device according to claim 20, which further comprises row decoders each provided for each of a plurality of word lines and in which said latch circuit is provided in each of said row decoders and generates and holds the word line activation signal for each of said row decoders.

23. A semiconductor storage device in which a plurality of word lines are activated together by causing each of the word lines which is once activated to hold the activated state through a plurality of successive word line selection cycles, comprising:

a function circuit which is configured to continuously hold redundancy hit information during a period in which a word line is selected and sets the defective word line into a non-selected state in a case where a corresponding word line once accessed is a defective word line.

24. The semiconductor storage device according to claim 23, wherein said function circuit is provided for each memory block.

25. The semiconductor storage device according to claim 24, wherein a plurality of signals each

containing the redundancy hit information is provided for each memory block.

26. The semiconductor storage device according to claim 23, wherein a signal containing the redundancy hit information is activated only in an operation mode which holds once activated word lines in the activated state during a plurality of successive word line selection cycles.

27. The semiconductor storage device according to claim 26, wherein timing for generating an output signal of an X decoder selected by an address is set later in the operation mode which holds once activated word lines in the activated state during a plurality of successive word line selection cycles than in the normal operation mode.

28. The semiconductor storage device according to claim 27, wherein the timing for generating an output signal of the X decoder selected by the address is set later in the operation mode which holds once activated word lines in the activated state during a plurality of successive word line selection cycles than in the normal operation mode by delaying a precharge release signal of a row decoder.

29. The semiconductor storage device according to claim 27, wherein the timing for generating an output signal of the X decoder selected by the address is set later in the operation mode which holds once activated

word lines in the activated state during a plurality of successive word line selection cycles than in the normal operation mode by delaying an address signal supplied to the X decoder.

30. The semiconductor storage device according to claim 25, wherein wirings used to transfer signals containing a plurality of redundancy hit information items are arranged on the same line without crossing each other.

31. A semiconductor storage device in which a plurality of word lines are activated together by causing each of the word lines which is once activated to hold the activated state during a plurality of successive word line selection cycles, comprising:

a latch circuit which is configured to derive the logical AND of a signal activated when a corresponding memory block is accessed and a redundancy miss is first made and a signal generated in each cycle to determine timing for activating a sense amplifier in each cycle, and generates and holds a sense amplifier activation signal.

32. The semiconductor storage device according to claim 31, wherein a plurality of word lines in the memory block are activated together.

33. A semiconductor storage device which has function of activating together a plurality of word lines connected to the same bit line pair via cell

transistors, comprising:

a column redundancy system which sets repair regions of column redundancy based on row addresses,

wherein the repair regions are set to permit the plurality of word lines activated together to belong to the same repair region when the repair regions are set to divide the bit line.

34. The semiconductor storage device according to claim 33, wherein the repair regions are set to cause the number of partial repair regions linked to configure one repair region to be suppressed to minimum.

35. The semiconductor storage device according to claim 33, wherein the repair regions are set to cause word lines which can be activated together in the memory cell array and used for reading/writing independent data simultaneously to belong to the same repair region.

36. A semiconductor storage device comprising:

a column redundancy system which sets repair regions of column redundancy based on row addresses,

wherein the repair regions are set to make maximum the number of word lines which can be activated together in one of the repair regions in an operation mode which holds once activated word lines in the activated state during a plurality of successive word line selection cycles under a condition that the scale

of the column repair region in a memory cell array is constant and the scale of each of partial repair regions linked to configure one of the column repair regions is constant or larger than the constant scale.

37. The semiconductor storage device according to claim 36, wherein the repair regions are set to cause word lines which can be activated together in the memory cell array and used for reading/writing independent data simultaneously to belong to the same repair region.

38. A semiconductor storage device comprising:

a column redundancy system which sets repair regions of column redundancy based on row addresses,

wherein the repair regions are set to make maximum the number of word lines which can be activated together in one of the repair regions in an operation mode which holds once activated word lines in the activated state during a plurality of successive word line selection cycles under a condition that the scale of the column repair region is constant and the number of repair regions which divide one bit line is constant or smaller than the constant number when the repair regions are set to divide the bit line.

39. The semiconductor storage device according to claim 38, wherein the repair regions are set to cause word lines which can be activated together in the memory cell array and used for reading/writing

independent data simultaneously to belong to the same repair region.

40. A semiconductor storage device comprising:

a column redundancy system which sets repair regions of column redundancy based on row addresses,

wherein the repair regions are set to make maximum the number of word lines which can be activated together in one of the repair regions in an operation mode which holds once activated word lines in the activated state during a plurality of successive word line selection cycles under a condition that the scale of the column repair region is constant, the scale of each of partial repair regions linked to configure one of the column repair regions is constant or larger than the constant scale and the number of repair regions which divide one bit line is constant or smaller than the constant number when the repair regions are set to divide the bit line.

41. The semiconductor storage device according to claim 40, wherein the repair regions are set to permit word lines which can be activated together in the memory cell array and used for reading/writing independent data simultaneously to belong to the same repair region.

42. A semiconductor storage device comprising:

a column redundancy system which sets repair regions of column redundancy based on row addresses,

wherein the repair regions are set to cause all of word lines which can be activated together in the operation mode which holds once activated word lines in the activated state during a plurality of successive word line selection cycles to belong to the same repair region.

43. The semiconductor storage device according to claim 42, wherein addresses are assigned in order from an upper address as far as possible as repair region setting row addresses.

44. A semiconductor storage device comprising:

a column redundancy system which sets repair regions of column redundancy based on row addresses,

wherein said column redundancy system has function of setting only defective word lines into a deactivated state in a case where a plurality of word lines among word lines activated together in the operation mode which holds once activated word lines in the activated state during a plurality of successive word line selection cycles are defective, selecting a plurality of spare word lines instead of the defective word lines, permitting the plurality of substituted spare word lines to be connected to the same bit line pair via cell transistors and setting only the spare word lines into a disable state.

45. The semiconductor storage device according to claim 44, further comprising another array for row

redundancy.

46. A column redundancy system which sets repair regions of column redundancy based on row addresses comprising:

a circuit which is configured to set only defective word lines into a deactivated state in a case where a plurality of word lines among word lines activated together in an operation mode which holds once activated word lines in the activated state during a plurality of successive word line selection cycles are defective and prevent spare word lines which are to be substituted for the defective word lines from being activated.

47. A method of testing a semiconductor storage device including a plurality of memory blocks, each in which a plurality of word lines can be activated together by holding once activated word lines in the activated state during a plurality of successive word line selection cycles and any defective word lines among a plurality of word lines word lines to be activated together can be selectively deactivated, said method comprising:

activating only one word line drive signal supplied to word line drivers; and

selecting a plurality of row decoders to activate a corresponding word line drivers by inputting different address at each cycle during a plurality of

successive word line selection cycles, and activating together a plurality of word line in a memory block.

48. A semiconductor storage device in which a plurality of word lines are activated together by holding each of the word lines which is once activated in the activated state during a plurality of successive word line selection cycles, comprising:

a memory array having a plurality of word lines; and

a spare cell array having a plurality of spare word lines which are provided to replace any one of the word lines, which is found to be defective,

wherein any one of the spare word lines, which has replaced a defective one of the word lines that are to be activated together during a plurality of successive word line selection cycles is activated by one word line drive signal.

49. A semiconductor storage device comprising:

a plurality of memory blocks;

word line drivers configured to drive the word lines provided in each of said plurality of memory blocks;

wires provided for each of said plurality of memory blocks;

array control circuits provided for each of said plurality of memory blocks, each of said array control circuits output a signal to control driving and

resetting of the word lines,

wherein signals output from adjacent two array control circuits are simultaneously supplied to both ends of a wire.